

Fabrication of two-dimensional photonic crystal waveguides for 1.5 μm in silicon by deep anisotropic dry etching

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Fabrication process for sharp waveguide bends in a two-dimensional photonic band gap structure in silicon is developed. The waveguide bend is defined by removing a row of pillars in a two-dimensional photonic crystal of 5 μm long, 205 nm diameter pillars placed on a square lattice with a pitch of 570 nm. To meet the severe nanotolerance requirements in such a device the SF₆/O₂ electron cyclotron resonance plasma process at reduced temperature is tailored to extreme profile control. The impact of main plasma parameters—i.e., temperature, oxygen/fluorine content, and ion energy—on the sidewall passivation process is unraveled in detail. Crystallographic orientation preference in the etch rate is observed. © 1999 American Vacuum Society.
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I. INTRODUCTION

In the last decade ongoing research has demonstrated the great potential of photonic crystal structures for unprecedented control of light propagation in broad range of novel optoelectronic devices. In this context efficient light guiding around sharp bends is an important issue for integrated planar optical devices for telecommunication and optical computing applications. Calculations on two-dimensional (2D) photonic crystal structures show that high transmission for 90° bends with virtually zero radius of curvature is feasible.¹ The basic 2D structure typically exists of an array of pillars or holes. Diameter of the individual element and the pitch of the array should be on the wavelength scale of interest. Recently, the sharp bend principle in 2D photonic crystal structures was demonstrated experimentally in an array of macroscopically assembled Al₂O₃ pillars for radiation in the millimeter wavelength regime.² The present work deals with the experimental realization of sharp bends in a 2D photonic structure for 1.5 μm wavelength operation in silicon. In view of the much smaller wavelength it requires high resolution lithography and deep anisotropic dry etching.

Search for photonic devices in the micron and submicron wavelength regime [infrared (IR) and near-IR] has been greatly intensified in recent years now that appropriate nanofabrication becomes more and more available. Most investigations deal with photonic structures in III–V compounds like GaAs,³ GaAs/AlGaAs,⁴ AlGaAs,⁵ GaAsP,³ and InP.^{6,7} Fabrication is achieved using chlorinated plasmas, either by reactive ion etching (RIE) or chemically assisted ion beam etching. Photonic operation is somewhat hampered by the limited vertical confinement due to a moderate etch depth. The Si material system, highly suitable for the IR wavelength regime, has attracted rather limited attention so far. Very steep and deep macroporous silicon structures for 5 μm

wavelength operation have been realised by Grüning *et al.*⁸ using a wet electrochemical process. An in-plane 2D transverse electric/transverse magnetic (TE/TM) beam splitter in a structured SiO₂/Si multilayer⁹ and photonic band gap microcavities in a Si waveguide for 1.5 μm wavelength have recently been reported.¹⁰

For the realization of sharp waveguide bends in a 2D photonic Si structure we first consider the design (Sec. II), to quantify tolerances in the lateral dimensions and provisions for the essential vertical photon confinement. After the experimental details (Sec. III) the patterning process development itself is considered in Sec. IV. It deals with tailoring the plasma-substrate interaction process for most stringent lateral dimension control over large etch depths. Strong evidence for crystallographic orientation preference in the silicon etch rate shows up under RIE conditions. The work is concluded with full device realization (Sec. V).

II. DEVICE DESIGN

The concept for our photonic crystal waveguide device is depicted in Fig. 1. Part (a) shows the physical design consisting of a square lattice array of Si pillars with a bend-like defect structure incorporated. The high refractive index of Si ($n=3.44, \epsilon=11.8$) results in a large photonic band gap for 1.5 μm TM (E field parallel to pillar) waves in such a structure, as shown in Fig. 1(b). These results have been calculated using the transfer matrix method of Pendry and MacKinnon.¹¹ The photonic gap is calculated for a range of values for the pillar radius (r) to pitch (a) ratio r/a . On the vertical scale the dimensionless angular frequency $\omega a/2\pi c$ is plotted, where ω is the angular frequency and c the velocity of light in vacuum. Areas enclosed by two adjacent curves are band gap areas, where no TM radiation can propagate through the crystal. The widest gap is observed for $r/a=0.18$ and a normalized center frequency $\omega a/2\pi c=0.38$. For this setting the waveguide bend manifests itself

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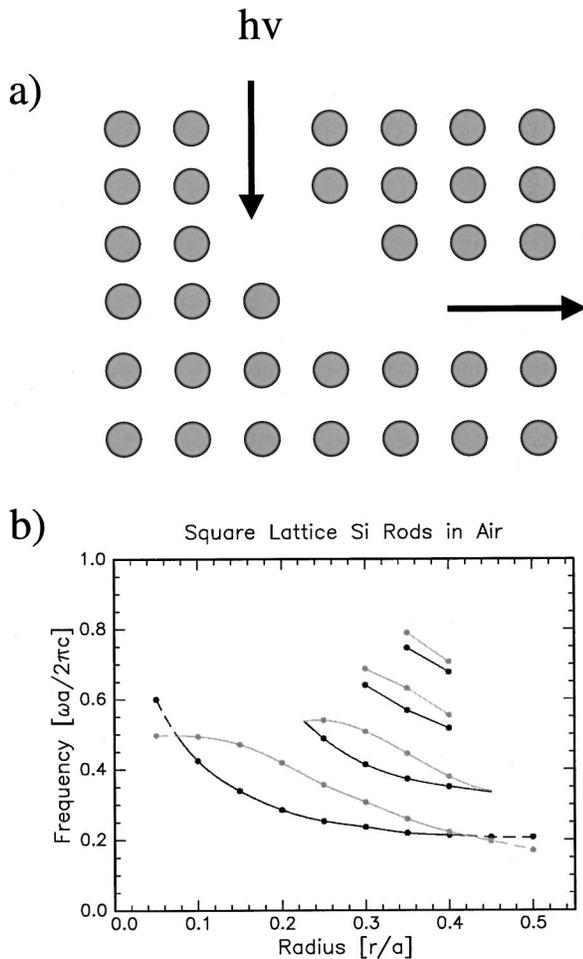


FIG. 1. (a) Design of photonic crystal waveguide bend in a square array of Si cylinders for optimal transmission viewed from the top and (b) photonic band gap for TM polarized waves as a function of the cylinder radius to pitch ratio r/a .

as a defect state in the center of the band gap. For $1.5 \mu\text{m}$ wavelength these calculations imply that the Si pillars should be each 200 nm in diameter on a pitch of 570 nm . To estimate the dimensional tolerances in the fabrication process one should consider two effects. First, for a fixed pitch of 570 nm the band gap exists roughly for $r/a = 0.18 \pm 0.04$, albeit increasingly smaller near the edges of the interval. Second, the position of the defect state in the gap for a fixed frequency shifts in a nonlinear way as a function of the r/a ratio.¹² Taking all together, we estimate r/a should be in the range 0.18 ± 0.02 . Keeping the pitch fixed (determined by the e-beam writing system within a few nanometers), the pillar diameter should be $205 \pm 23 \text{ nm}$.

For proper vertical confinement of the light the upper $1.9 \mu\text{m}$ of Si is taken to be amorphous ($a\text{-Si}$) instead of monocrystalline ($c\text{-Si}$), because $a\text{-Si}$ has a higher refractive index ($n = 3.75$). Calculations show that even with the $a\text{-Si}$ top layer pillars should be at least $5 \mu\text{m}$ high to avoid light leaking away into the $c\text{-Si}$ substrate. Taking lateral and vertical dimension requirements together pillar slope angles of

at least 89.3° for the upper $1.9 \mu\text{m}$ $a\text{-Si}$ part should be realized.

To ensure efficient light input and output ridge waveguides are positioned at both ends of the 2D bend structure. Calculations on a ridge type of waveguide show that the ridge should be 800 nm wide and 1200 nm deep in the $a\text{-Si}$ top layer for optimal monodisperse ground TM mode transmission. However, the different height of ridges and pillars implies a sequence of two anisotropic etching steps. An easier approach is to etch rectangular waveguides in a single step through the $a\text{-Si}/c\text{-Si}$ stack as deep as the pillars. A ridge width of 940 nm in front of the photonic waveguide opening suffices, however, at the drawback of allowing several higher TM modes besides the TM ground mode and possible losses due to sidewall roughness.

III. EXPERIMENT

The $a\text{-Si}/c\text{-Si}$ stack is obtained by amorphization of the top layer in $c\text{-Si}$ (100) substrates by implantation with 4 MeV Xe ions at 77 K at a dose of $2.10^{15} \text{ cm}^{-2}$ followed by an anneal at 500°C for 1 h to reach a thermally stable state with negligible absorption of $1.5 \mu\text{m}$ radiation. Transport of ions in matter calculations point to amorphization of the silicon down to 1750 nm depth and a maximal ion implantation depth of 2000 nm . After thermal anneal a $1.93\text{-}\mu\text{m}$ -thick $a\text{-Si}$ layer results as measured by ellipsometry in the $1200\text{--}1700 \text{ nm}$ wavelength range. Transmission electron microscopy analysis of Si-implanted samples shows the $a\text{-Si}/c\text{-Si}$ transition to be within 10 nm . Such a gradient has a negligible impact on the light confinement and photonic device operation.

Mask patterns are prepared either in thermal silicon oxide or in resist. Oxide mask on device samples should be grown prior to implantation to overcome the thermal budget limitation of $a\text{-Si}$ (550°C , 30 min). All samples are coated with a resist double layer consisting of 400-nm -thick bottom layer of hardbaked AZ S1813 photoresist (Shipley) with an overlying 80-nm -thick silicon containing negative tone e-beam resist-silicone based negative resist (Toyo Soda). After exposure (Leica EBPG05, 100 kV , $100 \mu\text{C}/\text{cm}^2$), development in xylene for 20 s followed by dipping in isopropyl alcohol for 30 s , the pattern is anisotropically transferred into the bottom photoresist layer by low pressure (0.3 Pa) oxygen RIE plasma at low radio frequency (rf) power density of $0.07 \text{ W}/\text{cm}^2$ [direct current (dc) bias of -170 V]. In case of an oxide mask an additional CHF_3 plasma at 0.8 Pa and $0.33 \text{ W}/\text{cm}^2$ rf power dc bias -260 V is applied. All patterning processes are *in situ* controlled by laser interferometry.

The Si etch process development is accomplished with a distributed electron cyclotron resonance (ECR) driven plasma setup (Alcatel DECR200), operating at 2.45 GHz , with He gas flowing at the back side of the substrate for appropriate temperature control (range $-150\text{--}150^\circ\text{C}$).¹³ The substrate is rf driven (13.56 MHz) for independent ion energy control towards the sample. Gas mixture is throughout SF_6/O_2 with the SF_6 flow fixed at 22.5 sccm at pressures

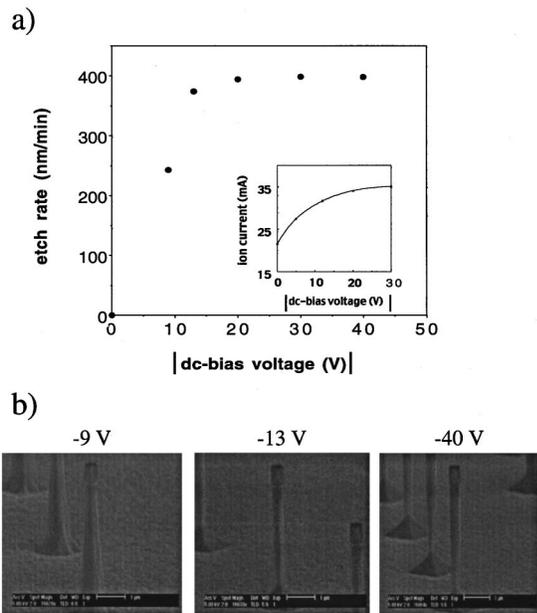


FIG. 2. (a) Si etch rate as a function of the substrate dc bias, with the other process parameters on their standard setting. The inset shows the ion current as a function of dc bias. (b) The resulting etch profiles. The 450 nm wide resist mask is still on top of the pillars.

around 0.2 Pa. Microwave power of 400 W is used unless stated otherwise.

Anisotropic etching in SF_6/O_2 high density plasmas (ECR driven¹⁴ or inductively coupled)¹⁵ can be taken as standard now. For the delicate sidewall passivation a strong coupling between the temperature and oxygen flow settings exists. Taking -80°C and 3 sccm O_2 as a start position, with the standard dc bias setting on -13 V , we focus on the plasma-substrate interactions required for extreme profile control. In this context temperature (range -105 – -65°C), oxygen flow (2–4 sccm), and dc bias (-50 – 0 V) are the most important parameters in the process development. Mask selectivity, both silicon oxide and resist, is almost infinite at these process conditions. It is pointed out that such a low ion energy at a long mean free path of centimeters accesses plasma-substrate interactions not available in RIE.

IV. PROCESS DEVELOPMENT

Figure 2 shows the etch rate [part (a)] and etch profile [part (b)] of individual *c*-Si nanopillars as function of the dc bias of the substrate electrode. In a separate inset the ion current towards the substrate as a function of dc bias is shown. The ion current plot indicates that beyond -20 V bias all positive ions available from the plasma are captured. After a sharp increase of the etch rate from 0 to 390 nm/min for increasing bias in the 0– -20 V region the rate saturates for higher voltages. The strong rate increase coincides with the increase of the ion current in the 0– -20 V bias region. Apparently, atomic fluorine is available in great excess and just ion flux (not the ion energy) is the etch rate limiting factor.

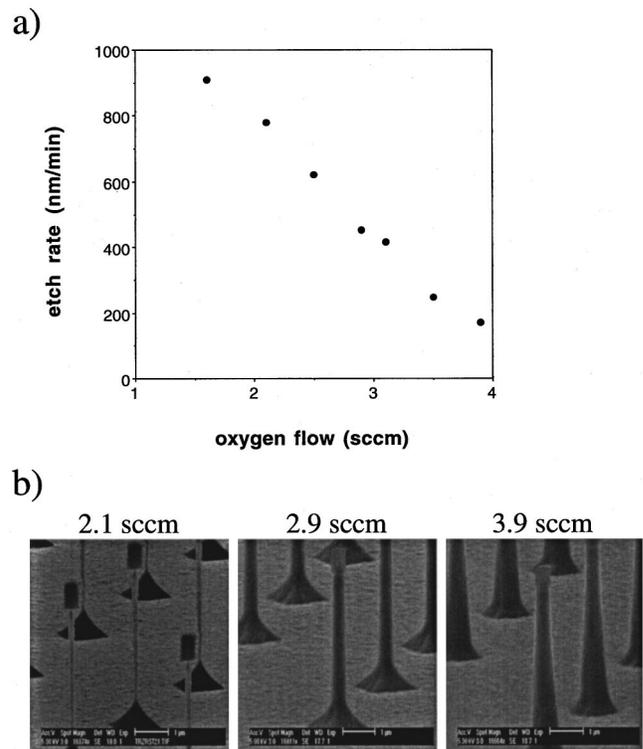


FIG. 3. (a) Si etch rate and (b) resulting etch profiles as function of the oxygen flow, with the other process parameters on their standard setting. The 450 nm wide resist mask is still on top of the pillars.

For increasing bias, the etch slope turns gradually from positive to negative. In view of the long mean free path (centimeters) compared to dark space thickness (around $100\ \mu\text{m}$) ion flux enters perpendicularly to the substrate. Ion deflection towards the sidewall¹⁶ cannot explain lateral erosion at increasing dc bias. In grating structures processed under the same process conditions we observed an increasingly negative slope for a larger clearing area around a given ridge. In the absence of spontaneous etching (there is negligible isotropic undercut) the negative slope is then probably due to ions scattered back from the horizontal surface.¹⁷ For effective etching/sputtering of siliconoxyfluorides at the sidewalls an energy threshold around 10–30 eV exists, i.e., in the same range but certainly lower than the threshold of 35 eV measured for silicon oxide.¹⁸ In separate x-ray photoelectron spectroscopy (XPS) inspections of surfaces etched at 0 and -20 V dc bias we indeed observed an increased removal of the lower (with less oxygen) oxyfluoride products at the higher bias. It is pointed out that the actual ion energy is larger than the dc-bias setting suggests because ions are accelerated from positive plasma potential region (on the order of $+10\text{ V}$). Finally, substantial facetting at the Si pillar footprint shows up. Anticipating results shown later, this observation is reminiscent of crystallographic orientation preference in the dry etch process.

Etch behavior of individual *c*-Si pillars as a function of oxygen flow is shown in Fig. 3. Rates [part (a)] sharply drop from 900 nm/min at 1.6 sccm to 180 nm/min at 3.9 sccm.

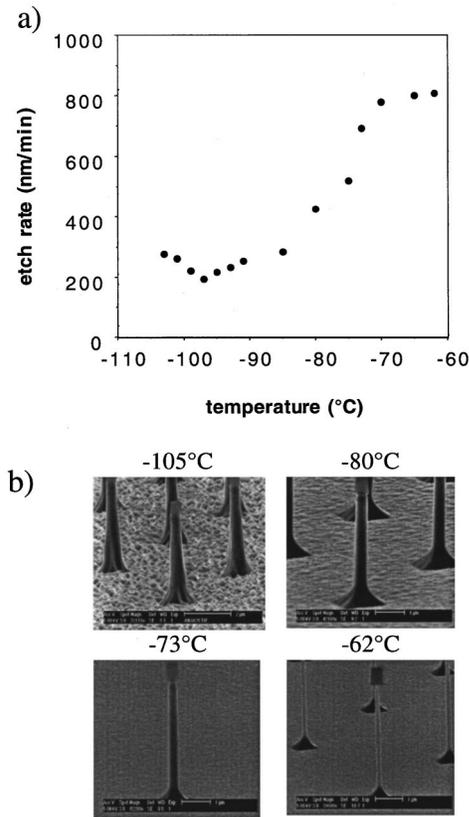


FIG. 4. (a) Si etch rate and (b) resulting etch profiles as function of temperature, with the other process parameters on their standard setting. The 450 nm wide resist mask is still on top of the pillars.

The large sensitivity is attributed to the moderate ion energy (dc bias -16 V) which is exactly in the range of the sputter thresholds of the oxyfluoride etch products. Part (b) shows etch profiles at different O_2 flows. At 3.9 sccm the tapered profile points to a significant sputter component. At 2.9 sccm profile is almost perfectly anisotropic probably because an ion-induced *chemical* etch component is most dominant. At 2.1 sccm the negative slope shows up again. Apparently, for smaller oxygen flow lower oxygen content in the sidewall oxyfluoride builds up and greater sensitivity for parasitic ion exposure results. However, a slight, more or less *homogeneous* (over the full height) lateral pillar narrowing is also observed. Moreover the faceting at the footprint has steadily increased for lower oxygen flows. Altogether the actual profile development is a combination of a vertical process and faceting at the footprint, on which is superimposed a slight lateral component which may be partly attributed to erosion from reflected ions.

Figure 4 shows the temperature behavior of the Si-pillar process in the range of -105 – -62 °C. After a continuous decrease towards lower temperatures [see part (a)] a minimum in etch rate is reached around -97 °C. The slight increase at even lower temperatures is unclear. At the lowest temperature the tapered profile without any underetch points to a process being highly sputter controlled. The horizontal surface is rough probably because oxidic condensates act as

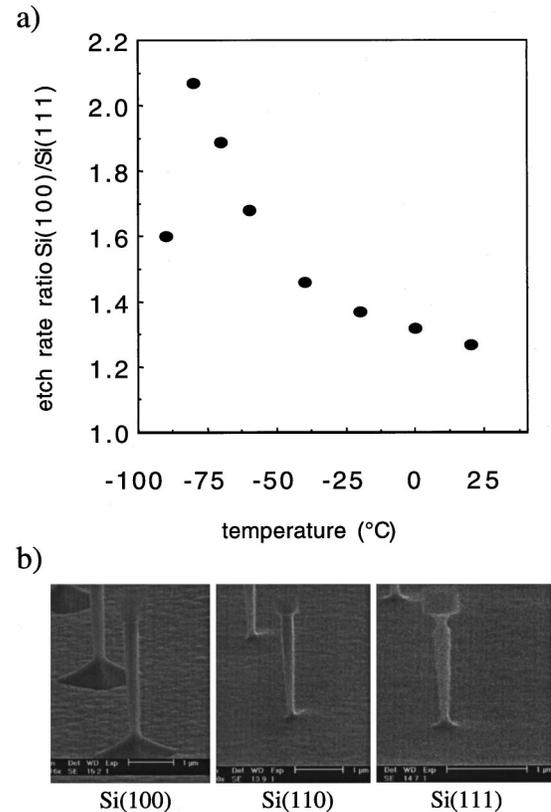


FIG. 5. (a) Comparison of the etch for different crystallographic orientations of the Si surface as a function of temperature. (b) Corresponding etch profiles.

a mask. On close inspection the rough surface predominantly consists of tiny pyramids suggesting the crystallographic preference noted previously. Profile behavior for increasing temperature is more or less the same as observed in the series for decreasing oxygen flow: an ion-induced *chemical* process, enhanced faceting at the footprint and at the highest temperature of -62 °C an observable homogeneous lateral pillar narrowing. At the latter temperature the sidewall starts to roughen possibly because sidewall passivation is hampered due to weak spots.

The substantial faceting at the footprint, homogeneous lateral narrowing, and pyramidal surface roughness prompts a more accurate look at crystallographic preferences. In Fig. 5 etch rates (a) and profiles (b) of different silicon orientations etched simultaneously in the same experiment are compared. Over a broad temperature range from -105 up to 20 °C the etch rate of Si(100) is larger than that of Si(111), with a maximum ratio of 2.04 at around -80 °C. The etch profiles for different Si orientations are revealing. In Si(111) and Si(110) the faceting at the footprint is absent; it is present in Si(100) because Si(111) planes are partly rate limiting. In both Si(111) and Si(110) the homogeneous lateral pillar narrowing is more pronounced. Si(111) shows by far largest initial undercut introduced at the start of the process in all samples (see Figs. 2, 3, and 4). All samples show the same negative slope from parasitic ions.

The higher etch rate of Si(100) agrees well with the XPS

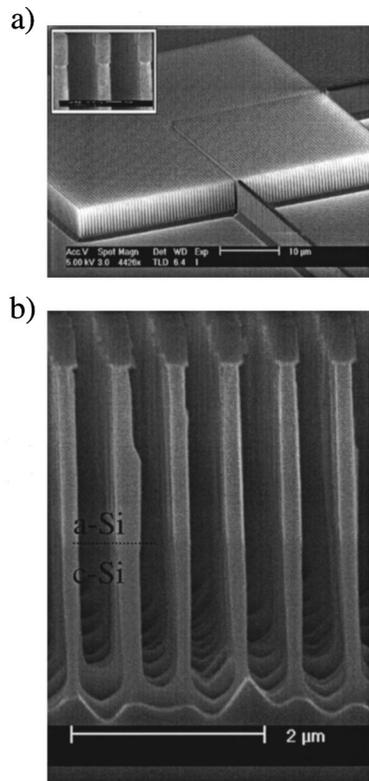


FIG. 6. Fabrication of 2D photonic waveguide bend in silicon for 1.5 μm wavelength light using 5 μm deep, 205 nm diameter rods on a pitch of 570 nm. (a) Full device with input and output waveguides, (b) profile behavior in $a\text{-Si}/c\text{-Si}$ double layer. A slight color contrast is observed between the $a\text{-Si}$ and $c\text{-Si}$ regions as indicated by the dashed line.

observation¹⁹ that at the Si(100) surface apparently more SiF_2 species evolve compared to Si(111) because of two and one dangling bonds per Si surface atom, respectively. SiF_2 is considered to be the essential intermediate etch species to form the SiF_4 end product in consecutive disproportionation reactions.²⁰ For etching of Si(111) along the SiF_2 intermediate state a Si-Si bond should be broken, with inherently a higher activation energy and thus resulting in a lower etch rate. We observed a significant increase by 20% in Si(100) etch rate from room temperature down to -65°C which like the minimum at -97°C cannot be explained yet. The lower desorption of etch species towards even lower temperatures is clearly overruled by a more efficient rate limiting step in the overall etch mechanism.

V. DEVICE FABRICATION

2D photonic waveguide bend structures for 1.5 μm wavelength in Si are dry etched with our ECR plasma of SF_6/O_2 (7.3:1) at 0.1 Pa pressure, -97°C substrate temperature, 400 W μwave power, and -12 V dc bias, at a rate of about 150 nm/min. The results are summarized in Fig. 6. The full device is depicted in Fig. 6(a) showing an array of 205 nm wide and 5 μm high $c\text{-Si}$ pillars in Si(100). Aspect ratio is about 50. The homogeneous pillar width is shown in the inset. The uniform etch depth agrees with the rate limiting step being related to surface kinetics rather than limited by

in- and outdiffusion of the reactive species in the deep etched cavities. We also tested the etch process for the $a\text{-Si}/c\text{-Si}$ stack. A typical result is shown in Fig. 6(b). The slight grey-tone transition (indicated by dashed line) is reminiscent to the $a\text{-Si}/c\text{-Si}$ interface as its position corresponds to the expected depth (see Sec. C. III). The $c\text{-Si}$ bottom part of the pillars tends to a slightly negative slope, while the $a\text{-Si}$ part is almost perfectly anisotropic. The $a\text{-Si}$ layer has a 30% lower etch rate than $c\text{-Si}$. Given the oxygen flow results shown in Fig. 3 both profile and rate observations can be explained by the buildup of a slightly higher oxygen content in etched surface and sidewalls of $a\text{-Si}$. In the crossover at the $a\text{-Si}/c\text{-Si}$ interface the oxyfluoride balance on both horizontal surfaces and sidewalls shifts then to a lower oxygen content and so to enhanced sensitivity to ion exposure. For a more quantitative understanding XPS measurements of the O/F ratio in the sidewall passivation under the various process conditions is underway, as was previously done for SiGe.²¹

VI. CONCLUSIONS

A fabrication process for photonic band gap structures in Si has been developed using ECR driven SF_6/O_2 plasma at reduced temperature. Very high control in the sidewall profile is achieved. Depending on the actual setting of ion energy (by virtue of dc bias), fluorine/oxygen ratio and substrate temperature the etch profile can varied from positively to negatively sloped. The latter is attributed to the impact of ions reflected from the horizontal surface. At the low ion energies used (0–50 eV) crystallographic orientation preference in the Si etch rate shows up which seems intimately related to the different ability of Si(100) and Si(111) to yield SiF_2 species as the key intermediate etch product. The surface-kinetics controlled etch behavior enables extreme profile control up to aspect ratios of 50, meeting the severe requirement for sharp photonic waveguide bend applications in silicon. Device characterization is underway and will be reported in due course.

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